UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,055	11/29/2001	Dominik Zeiter	PHCH000025 US	5505

24737 7590 05/05/2004

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2673	8

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,055	ZEITER ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will ba considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause tha application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 6.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other. _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (US Patent No. 6,426,594 B1) in view of Imai et al. (US Patent no. 6,256,025 B1), Hartung et al. (US Patent No. 5,859,625).

As to claims 1, Ito teaches a display device which includes a driver circuit (See Fig. 3, items 31-35, in description See Col. 20, Lines 11-15) and display with a plurality of rows and columns (See Fig. 5, items X1-Xm, Y1-Yn, in description See Col. 14, Lines 2-10), where a number p indicates the number of simultaneously driven rows (See Figs. 1,5, in description See Col. 14, Lines 48-52), where the rows and columns can be driven by means of voltage values of the equally high voltages (See Fig. 6, items V2,-V2, in description See Col. 5, Lines 1-6 and Col. 15, Lines 7-20), wherein the display device derives the number p of simultaneously driven rows from the display size to be driven, and is configured to adaptively select number p of simultaneously driven rows in response to a change in a display mode that controls the display size to be driven: four lines for 120 scanning electrodes and three voltage levels in total (See Fig. 1,5-6, in description See Col. 14, Lines 48-52 and Col. 16, Lines 9, 22-23) and seven lines for 203 scanning electrodes and five voltage levels in total (See Fig. 7-8, in description See Col. 22, Lines 22-26, Col. 25, Lines 23-26 and Col. 26, Lines 1-4).

Ito does not show the driver circuit includes plurality of voltage driver stages for

generating corresponding partial voltage values for driving the display and selected number p of simultaneously driven rows such that the number of partial voltage values that are available for driving the display during the display mode varies in dependence on number p of simultaneously driven rows selected for the display mode.

Imai et al. teaches the driver circuit includes plurality of voltage driver stages for generating corresponding partial voltage values for driving the display (See Fig. 2, items 21-23, Col. 7, Lines 14-23) and selected number p of simultaneously driven rows such that the number of partial voltage values that are available for driving the display during the display mode varies in dependence on number p of simultaneously driven rows selected for the display mode (See from col. 7, Line 67 to Col. 8, Line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement the driver circuit includes plurality of voltage driver stages for generating corresponding partial voltage values for driving the display and selected number p of simultaneously driven rows defines the number of the voltage values as shown by Imai et al. in the Ito apparatus in order to provide a low-priced voltage generating circuit capable of switching and outputting voltages at plural levels with low power consumption (See Col. 3, Lines 15-20 in the Imai et al. reference).

Ito and Imai et al. do not show selectively switching off driver voltage stages.

Hartung et al. teaches show selectively switching off driver voltage stages in response to changing mode (See Figs. 1, 3-4, items 130, 140, 150, Col. 6, Lines 26-44 and Col. 4, Lines 26-32).

It would have been obvious to one of ordinary skill in the art at the time of invention to

selectively switching off driver voltage stages in response to changing mode as shown by Imai et al. in the Ito and Imai et al. apparatus in order to achieve the smallest possible average power drain (See Col. 2, Lines 37-38 in the Hartung et al. reference).

Notice that, multiplexibility (m) is inherently defined as maximum number of multiplexed (switchable) rows (R). Therefore, m >= R.

As to claim 4, Tamai et al. teaches the optimum value p of rows to be simultaneously driven as derived from the display size that is smaller than the maximum value (See Fig. 1, items 1-2, Col. 2, Lines 26-31 and Col. 4, Lines 23-25).

2. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito, Imai et al. Hartung et al. as applied to claim 1 above, and further in view of Tamai et al. (US Patent no. 6,346,774 B1).

As to claim 2, Ito, Imai et al. Hartung do not show the optimum number p of rows to be simultaneously driven as derived from the display size.

Tamai et al. teaches the optimum number p of rows to be simultaneously driven as derived from the display size (See Fig. 1, items 1-2, in description See Col. 2, Lines 26-31 and Col. 4, Lines 23-25).

It would have been obvious to one of ordinary skill in the art at the time of invention to use Tamai et al. approach in the Ito, Imai et al. Hartung apparatus in order to reduce the number of levels associated with the driving voltage and reduce total power consumption (See Col. 9, Lines 1-7 in the Ito reference).

As to claim 3, Ito, Imai et al. Hartung do not show a sequence for the supply of the image data to be displayed from a memory is the same for all values p.

Tamai et al. teaches a sequence for the supply of the image data to be displayed from a memory is the same for all values p (See Fig. 1, items 5-6, in description See Col. 7, Lines 58-63).

It would have been obvious to one of ordinary skill in the art at the time of invention to use Tamai et al. approach in the Ito, Imai et al. Hartung apparatus in order to reduce the number of levels associated with the driving voltage and reduce total power consumption.

3. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito in view of Imai et al. and Hartung et al.

Ito teaches a driver circuit (See Fig. 3, items 31-35, in description See Col. 20, Lines 11-15) and display with a plurality of rows and columns (See Fig. 5, items X1-Xm, Y1-Yn, in description See Col. 14, Lines 2-10), where a number p indicates the number of simultaneously driven rows (See Figs. 1,5, in description See Col. 14, Lines 48-52), wherein the display device derives the number p of simultaneously driven rows from the display size to be driven: four lines for 120 scanning electrodes and three voltage levels in total (See Fig. 1,5-6, in description See Col. 14, Lines 48-52 and Col. 16, Lines 9, 22-23) and seven lines for 203 scanning electrodes and five voltage levels in total (See Fig. 7-8, in description See Col. 22, Lines 22-26, Col. 25, Lines 23-26 and Col. 26, Lines 1-4).

Ito does not show the driver circuit includes plurality of voltage driver stages for generating corresponding partial voltage values for driving the display and selected number p of simultaneously driven rows that is derived therefrom.

Imai et al. teaches the driver circuit includes plurality of voltage driver stages for generating corresponding partial voltage values for driving the display (See Fig. 2, items 21-23, Col. 7, Lines 14-23) and selected number p of simultaneously driven rows that is derived therefrom (See from col. 7, Line 67 to Col. 8, Line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement the driver circuit includes plurality of voltage driver stages for generating corresponding partial voltage values for driving the display and selected number p of simultaneously driven rows defines the number of the voltage values as shown by Imai et al. in the Ito apparatus in order to provide a low-priced voltage generating circuit capable of switching and outputting voltages at plural levels with low power consumption (See Col. 3, Lines 15-20 in the Imai et al. reference).

Ito and Imai et al. do not show selectively switching off driver voltage stages.

Hartung et al. teaches show selectively switching off driver voltage stages in response to changing mode (See Fig. 1, item140, Col. 6, Lines 30-32).

It would have been obvious to one of ordinary skill in the art at the time of invention to selectively switching off driver voltage stages in response to changing mode as shown by Imai et al. in the Ito and Imai et al. apparatus in order to achieve the smallest possible average power drain (See Col. 2, Lines 37-38 in the Hartung et al. reference).

Response to Amendment

4. Applicant's arguments filed on 02-17-04 with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

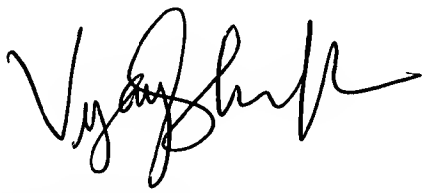
Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ls



VIJAY SHANKAR
PRIMARY EXAMINER